STUDIES ON MOS OXIDE FORMATION AND SCALED MOS DEVICES(MOS酸化膜形成とスケールダウンMOSデバイスの研究)

氏名	角南英夫（すなみひでお）
授与学位	工学博士
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論文審査委員	東北大学教授 西沢 潤一　東北大学教授 松尾 正之 東北大学教授 御子柴宣夫

論文内容要旨

Since the first MOS (Metal－Oxide－Semiconductor) integrated circuit appeared in 1963, there has been very rapid progress in the number of devices per chip. As a result, four times greater integration in MOS memory has been accomplished every three years resulting in a development of present 256 Kb dRAM.

The objectives and contents of this thesis are to study physical properties and formation techniques of oxide films widely used in silicon LSI's associated with their applications to MOS LSI's and realized performances of MOS devices scaled down to the 1 μm level, particularly concerning;

(1) stress behaviors of insulating films and their applicability to multi－level interconnections,

(2) enhanced oxidation of heavily doped polysilicon and its application to;

(3) double－polysilicon gate MOS structure and highly self－aligned device fabrication, and,

(4) experimental clarification of limiting factors in device down scaling.

Stress behaviors of chemical－vapor－deposited (CVD) insulating films deposited on Si substrate revealed that the room temperature stress ranged from

2×10^8 to 4×10^9 dyn/cm^2 (tensile), as shown in Fig. 1, and the stress in the CVD SiO_2 film was reduced significantly by moisture absorption. After 600°–900°C heat treatment, which led to densification, the room temperature stress became compressive, as shown in Fig. 2, and the stress reduction due to the moisture absorption was no longer observed.

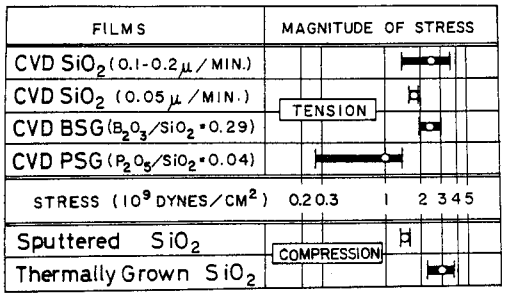

Fig. 1 Room temperature stresses in films deposited on (111) Si wafers.

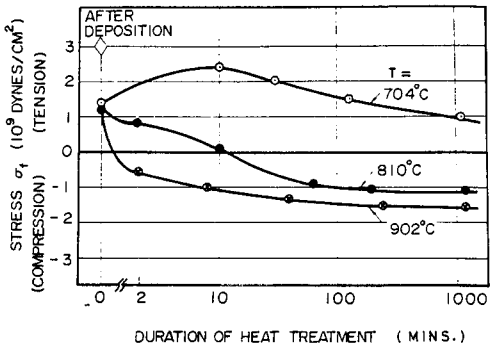

Fig. 2 Room temperature stress changes in CVD SiO_2 after heat treatments in nytrogen.

Stress measurements by the Newton ring method at elevated temperatures up to 750°C provided a direct evaluation of thermal expansion coefficient and elastic constant, and the intrinsic stress generated during the film deposition. The intrinsic stresses, speculated to be caused by porous structure of the film, were found tensile for all CVD films. While, they were too little to be observed for thermal and sputtered SiO_2 films. Concerning the stress behavior and the alkali-ion gettering capability, a CVD phosphosilicate (PSG) film was applied to multi-level interconnection as an intermediate insulating film.

The enhanced oxidation effects, previously observed in the oxidation of heavily doped single Si, has been extended to phosphorus-doped poly-Si in the temperature range from 700° to 900°C. The enhancement was pronounced for P-concentration above 1×10^{20} cm^{-3} as shown in Fig. 3. Moreover, above P-concentration of 1×10^{21} cm^{-3}, a very rapid oxidation took place at the beginning of the oxidation resulting in "initial oxide" which was found to be P-rich SiO_2 from SIMS measurements. Oxide thickness x^2 vs oxidation time t plots in Fig. 4 clarify the existence of the initial oxide.

The aspect of the enhanced oxidation of heavily doped poly-Si had great impacts on double poly-Si MOS structure formation and highly self-aligned device fabrication.

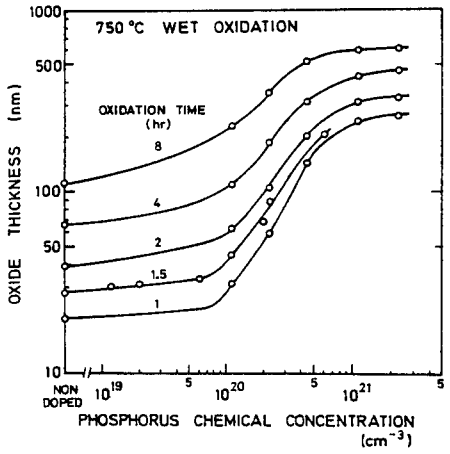

Fig. 3 Thermal oxidation of phosphorus doped polycrystalline Si at 750°C in wet oxygen.

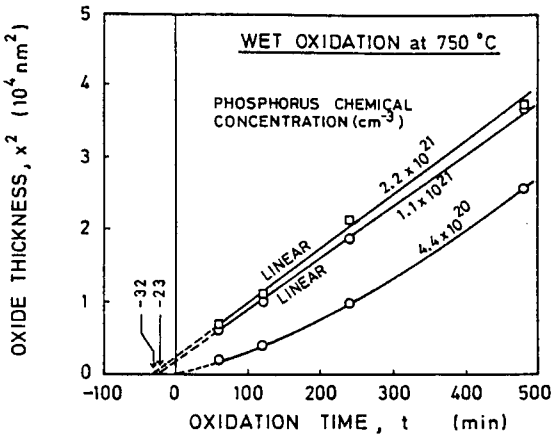

Fig. 4 Oxide thickness x^2 vs oxidation time t plots for revealing the existence of "initial oxide".

A thick intermediate oxide between the first and the second poly-Si gates and a thin second gate oxide were formed with a simultaneous wet oxidation leading to considerable improvements in dielectric breakdown field strength of the oxide and a reduction of a few processing steps. This technique is named SELOCS (SELective Oxide Coating of Silicon Gate). Cross-sectional configurations and the improvement are shown in Figs. 5 and 6, respectively, for the conventional CVD and SELOCS methods.

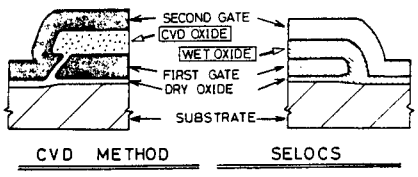

Fig. 5 Cross-sectional configurations of the conventional CVD and SELOCS structures.

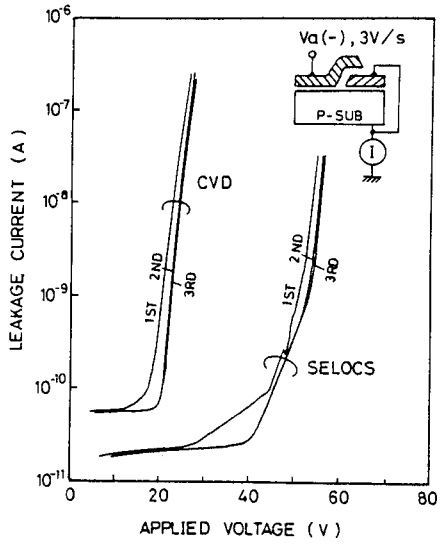

Fig. 6 Leakage current improvement by SELOCS method.

Despite favorable device and circuit performances, substantial limitation in intermediate oxide thickness was found to exist. Excessive oxidation in thickness

produced an overhang which caused anomalously thin intermediate oxide and fatal electrical shorts. Guiding principles affecting the overhang formation were discussed in terms of oxidation conditions concerning cross-sectional configuration and oxidation kinetics. According to guiding principles established, dry-wet-dry (D-W-D) oxidation was successfully developed.

In addition to the intermediate oxide formation, a novel self-aligned MOS device has been developed utilizing SELOCS. A process sequence is shown in Fig. 7. Since the entire surface of poly-Si gate was uniformly covered with its own oxide, this SELOCS technique provides nearly zero registration margin between the photoengraving of source and drain contact holes and the gate resulting in almost doubling of packing density without requiring finer patterning technology. To realize satisfactory dielectric breakdown voltage, some improvements are still required for LSI-level fabrication.

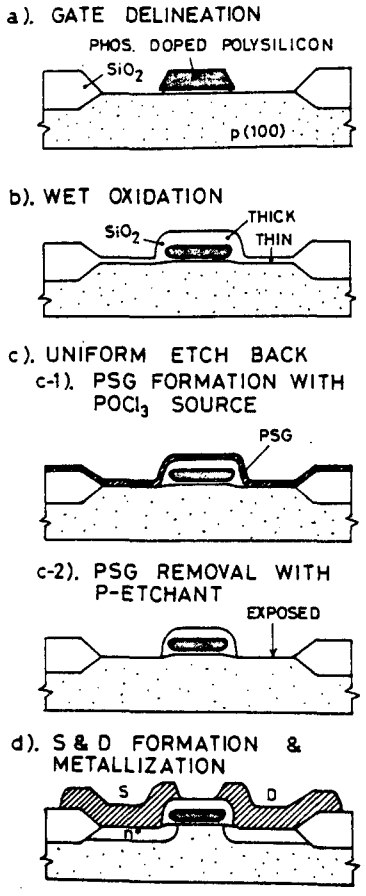

Fig. 7 Process sequence for self-aligned contacts to source and drain.

Projected three levels of scaled MOS devices envisioned in the next decade have been experimentally characterized in terms of device performances such as threshold voltage definition, source to drain breakdown behavior and effective electron mobility reduction. The final third-level device had 20 nm thick gate oxide and 0.7 μm channel length on an assumption that one level provides a scaling ratio of 0.7. Structural parameters of the devices investigated are shown in Table 1.

Table 1 Structural parameters

SYMBOLS	ρ_{sub} (Ω-cm)	T_{ox} (nm)	N_{dose} (cm^{-2})	X_j (μm)
⓪	10	50	5×10^{11}	0.48
①	10	35	7×10^{11}	0.30
②	10	25	1×10^{12}	0.30
③	4	20	1×10^{12}	0.18

Threshold voltage V_{TH} vs effective channel length L_{eff} curves and g_m/C_g values designating circuit speed are shown in Figs. 8 and 9. respectively, for four scaling levels.

Among various limitation factors in device down scaling, most serious problems have been found to be (a) source to drain breakdown which has a close relation to hot electron trapping and (b) acceleratedly increased failure rates in oxide integrity corresponding to the oxide thickness reduction. Two or three dimensional designing of impurity profiles in substrate and S and D structures and reliable gate insulators should be developed to break through the problems cited above.

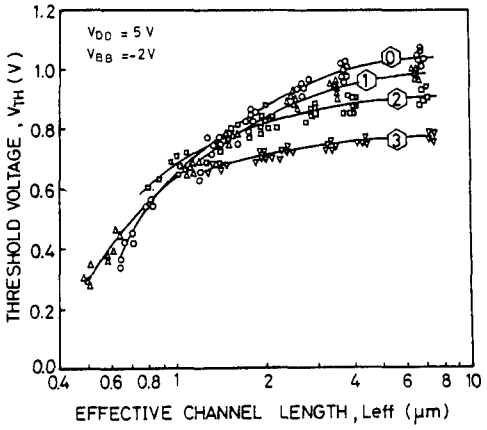

Fig. 8 Short channel effects on V_{TH} for four levels.

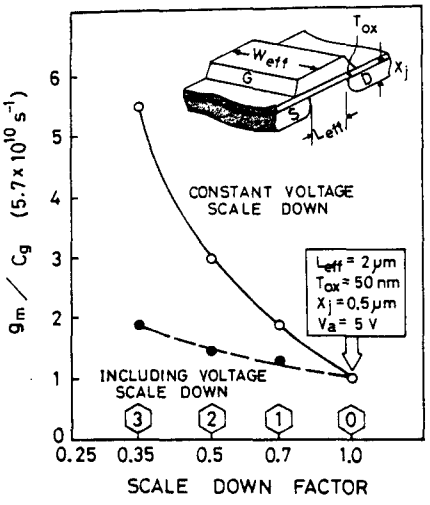

Fig. 9 Evaluated circuit perfomance g_m/C_g values designating circuit speed using transistor performances experimentally obtained.

審 査 結 果 の 要 旨

半導体の表面を酸化して形成した絶縁膜上に金属などの導電電極を接着し，その電極に電圧を加え，半導体表面部分の導電率を静電誘導効果によって変化させるMOS技術は，今日半導体集積回路（IC）の二大主流のうちの一つの方向（MOSIC）の基礎技術である。

特に一つのシリコン基板に1000個以上の素子を作り込んだ大規模集積回路（LSIIC）では，酸化物膜の形成加工技術の再現性と信頼度がその死命を制する。また，将来どこまで高密度集積が可能になるかについても，どこまで微細化ができるかに依存する部分が多い。本研究は，それらの基礎となるシリコン表面に形成した酸化物膜が内蔵する機械的応力のふるまいと，それをある限度内に収め，高密度集積技術に実用できるようにするための基礎データを中心としてまとめたもので，本文7章と付録2章よりなる。

第1章は序文で，本研究の背景をのべたものである。第2章では，シリコン結晶表面に酸化物膜を形成したときに起こる結晶板の球面変形を測定する方法と，この歪の測定から内蔵する機械的応力の算定のしかた及び膜の形成条件による変化についてのべている。

第3章では，最近，多結晶シリコン膜を気体中で酸化する場合にも，気体中に燐成分を同時に送り込むことによって高速酸化ができる現象を応用する傾向にあるが，この重要技術の基礎を明らかにするために，単結晶とイオン注入結晶，多結晶膜について実験を行い，反応速度論的に解析し，有用な諸量を求めると共に種々考察を加えている。

第4章では，前章までの結果に基づいて，シリコン単結晶表面に形成された酸化物膜の上に多結晶シリコンでゲートを形成するときに不純物の含有量を多くし，次の酸化物膜を形成する工程で厚い膜が選択的に形成されるようにしても，もれ電流の少ないMOS構造を形成することに成功したことを実測結果に基づいて示している。

第5章では，前章の技術によって形成される多結晶シリコン部分の位置ずれが，充分LSIICに実用できる程度のものであることを示している。

第6章では，以上の結果に基づいて超LSIの実現性について論じており，チャンネル長0.7 μmも可能であると推定している。第7章では，今後の問題点について種々のべている。付録は電荷転送デバイス，及び2次元結晶成長が欠陥によって妨げられて凹みを生ずることについてのべたものである。

以上要するに，本研究は半導体集積回路の重要基礎技術である酸化物膜の形成についてまとめたもので，半導体工学及び固体反応について多くの知見を加えており，電子工学に資するところが少なくない。

よって，本論文は工学博士の学位論文として合格と認める。